WHAT IS CLAIMED IS:

1. A system that substantially eliminates glitch comprising:

first and second drivers configured to receive first and second respective digital signals and generate first and second respective drive signals therefrom, the first and second drivers coupled between first and a second nodes; and

first and second switches configured to receive respective ones of the first and second drive signals and generate first and second respective analog signals therefrom,

wherein a difference in power signal values received at respective ones of the first and second nodes is set to a predetermined amount, such that a glitch in the first and second analog signals is substantially eliminated.

2. The system of claim 1, wherein:

the first and second switches are p-type transistors biased using a power supply.

3. The system of claim 2, wherein:

the first node receives a power signal having a value lower than the power supply; and

the second node is coupled to ground.

4. The system of claim 1, wherein the first and second switches are n-type transistors biased via a node coupled to ground.

SKGF: 1875.5070000/ BP 3173

5. The system of claim 4, wherein:

the first node receive a power signal from a first voltage source;

and

the second node receives a power signal from a second voltage source.

- 6. The system of claim 1, wherein the difference between the power signal values received at the first and second nodes determines respective swing values in the first and second drive signals.
- 7. The system of claim 6, wherein the swing values limit charge stored in the first and second switches.
 - 8. A method for substantially eliminating glitch comprising:

coupling first and second drivers between first and second nodes receiving first and second power supply values, such that a swing value in respective first and second drive signals is limited; and

driving respective first and second switches with the first and second drive signals to produce first and second respective analog signals,

wherein the limit in the swing value in the drive signals substantially eliminates glitches in first and second analog signals.

9. The method of claim 8, further comprising:

coupling the first node to a first voltage source that generates the first power supply value; and

coupling the second node to a second voltage source that generates the second power supply value, wherein the first and second voltage sources have different voltage values.

10. The method of claim 8, further comprising using the limiting of the swing values to limit stored charge in the first and second switches.

SKGF: 1875.5070000/ BP 3173

11. A method for substantially eliminating glitch comprising:
coupling first and second drivers between ground and a power
supply, such that a swing value in respective first and second drive signals is
limited; and

driving respective first and second switches with the first and second drive signals to produce first and second respective analog signals,

wherein the limit in the swing value in the drive signals substantially eliminates glitches in first and second analog signals.

12. The method of claim 11, further comprising using the limiting of the swing values to limit stored charge in the first and second switches.

SKGF: 1875.5070000/ BP 3173